High Performance Data Processor
(HPDP)

Payload
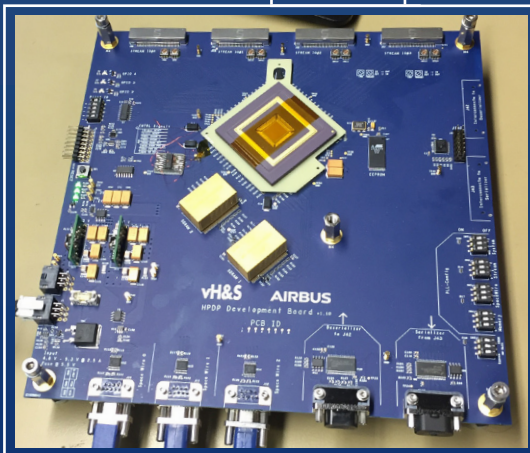
The High Performance Data Processor is a building block for very high reliability, radiation hard data processing. It is characterized by the ability to sustain a high data throughput combined with a high performance level and the flexibility to adapt target applications to emerging standards and improvements.

The potential of the HPDP lies in the processing capability of high data volumes in the signal-processing domain, especially where flexibility and in-orbit re-programmability or reconfiguration is required.

KEY FEATURES OF THE HPDP BOARD

- Based on XPP III Array Processor from PactXPP Technologies providing 40 Giga operations per second (End-of-Life)
- 4 Mbyte on-chip SRAM
- 5Gbit of on-board SDRAM
- Streak observations algorithms to detect space debris:
- - HPDP outperforms Desktop PC by factor 12
- Moon Asteroid Strike + Vessel Detection
- Performance of the implementation exceeds the required 1kfps
- Autonomous Navigation for Lander Units and Rovers
- RGB to Greyscale, Filtering and Corner detection within 4 ms
- 4 x 1.1 Gbit/s Streaming Ports compatible with HSSL

- Fully reprogrammable platform
- 3 SpaceWire interfaces for monitor and control operating at 100 Mbps on each channel with routing capability

MAIN APPLICATION FIELDS

- High Performance Processing (e.g. Image Processing)
- Low power Data Processing Unit
- Application Implementations (exemplary@250 MHz)

AIRBUS

CHARACTERISTICS OF HPDP-40 CHIP

40 ALU Processing Array (PAEs), arranged in a rectangular array, featuring:

- 40 ALU Processing Array Elements (PAEs 16-bit) running with 250MHz each
- 2 Harvard type VLIW 16-bit processor cores (FNCs) running at 125MHz
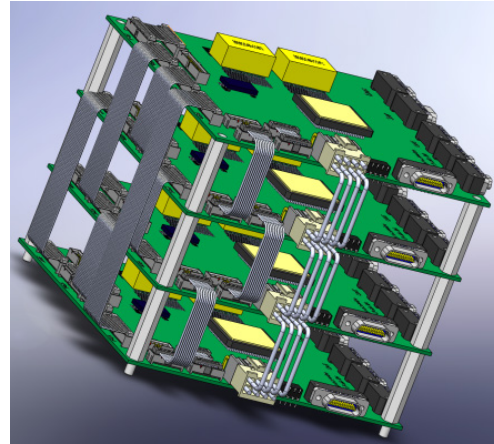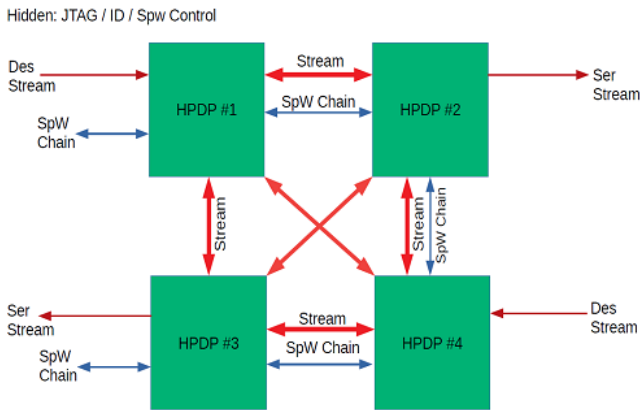- 256 Kbit high speed on-chip RAM

Fully radiation hardenend processor platform:

- Based on STM Rad hard 65nm CMOS technology platform for space applications (ITAR free)
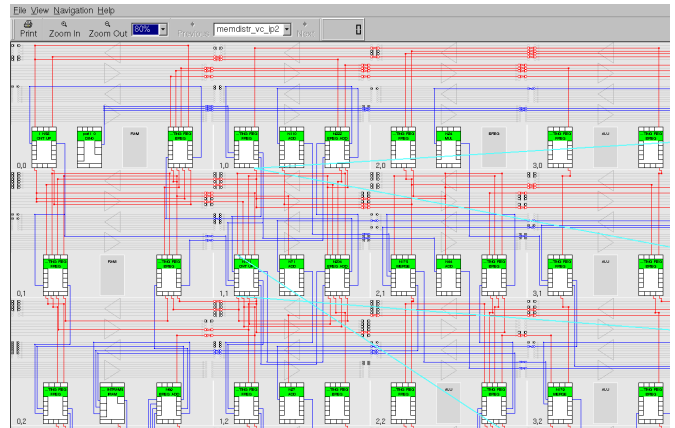
Environmental Operation conditions:

Temperature	-55 °C to +125 °C
TID Tolerance	>100 kRad
Single Event Latch-up Immunity	up to 60Mev/mg/cm2 at 125°C
Life Time in-orbit:	20 years

CASCADING OF HPDP BOARDS

SOFTWARE SUPPORT

- Software Debug Interfaces:
  - Run-time JTAG Debug Support Interface for register access and array debugging
  - Software upload and software monitoring via SpaceWire
  - Multi-chip simulation environment available
- Example algorithm implementations available
- GNU C-compiler and assembler tool targeted for the HPDP processor cores and array elements (FNC-PAEs).
- Stand-alone simulator for the FNC-PAEs
- Editor and NML code compiler for the HPDP Array.
- HPDP Array visualizing tool for the HPDP application developer (see snapshot).
- Multi-chip simulator

CHARACTERISTICS OF HPDP-40 CHIP

With or Without External RAM

A 512FFT on a LEON processor takes ~40K cycles
HPDP is a factor ~10 more efficient